REMARKS

Applicants thank the Examiner for the thorough consideration given the present application.

Claims 1-14 are pending in this application. Claims 1, 6, 9, and 14 are independent and are amended.

Reconsideration of this application, as amended, is respectfully requested.

Drawings

It is respectfully submitted that the formal drawings filed with the present application comply with USPTO requirements, and the Examiner is requested to provide a Notice of Draftsperson's Patent Drawing Review, Form PTO-948, confirming approval of the formal drawings with the next official communication.

Claim for Priority

The Examiner has acknowledged Applicants' claim for foreign priority under 35 U.S.C. §119 and receipt of the certified copy of the priority document.

Rejections under 35 U.S.C. §102(b) and §103(a)/Allowable Subject Matter

Claims 1-3, 5, 7, 8, 10, 12, and 13 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,995,189 to Zhang. Claim 14 is rejected under 35 U.S.C. §103(a) as being unpatentable over Zhang in view of

U.S. Patent No. 6,400,438 to Noritake et al., and claim 4 is rejected as being unpatentable over Zhang in view of U.S. Patent No. 5,945,984 to Kuwashiro. These rejections are respectfully traversed.

Claims 6, 9, and 11 are objected to as being dependent upon a rejected base claim would be allowable if rewritten in independent form including the limitations of the base claim and any intervening claims.

Claims 6 and 9 are amended to present indicated allowable subject matter in independent form. Claim 11 is not rewritten in independent form at this time.

While not conceding the appropriateness of the rejections, but merely to advance prosecution of the instant application, independent claim 1 is amended to recite a combination of elements in a liquid crystal device, including a sealant between upper and lower substrates in an area near an edge of the upper substrate, and a source PCB and a gate PCB electrically connected with pluralities of source pads and gate pads, respectively, the source PCB and the gate PCB being formed outside the area in which the sealant is formed such that the upper substrate is not formed over the source PCB or the gate PCB.

Independent claim 14 is amended to recite a combination of steps in a method of fabricating a liquid crystal display device, including forming a plurality of gate lines, gate pads, gate transmitting wires, and dummy patterns on the first substrate; forming a gate insulating layer on the gate lines, gate

pads, gate transmitting wires, and dummy patterns; forming a plurality of data lines and data pads on the gate insulating layer; and forming a passivation layer on the data lines and the data pads.

It is respectfully submitted that the combinations of elements and method steps set forth in independent claims 1 and 14 are not anticipated or made obvious by the prior art of record, including Zhang, Noritake et al., and Kuwashiro.

In contrast to Applicants' claimed invention, Zhang shows a signal line drive circuit 103 and a scanning drive circuit 104 located in an area surrounded by sealing material region 107 and, therefore, underneath an upper substrate, as shown in FIG. 1. An external terminal 108 on the substrate 101 is connected with the signal line drive circuit 103 and scanning drive circuit 104 through wirings 109. The structure taught by Zhang is very different from that of the present invention, because in the present invention the source PCB and gate PCB are both located outside the area that is enclosed by the sealant, and there is no need for an external terminal in the present invention. Furthermore, Zhang does not teach or suggest transmitting wires formed across a sealant such that they are protected by an upper substrate.

With respect to the rejection of claim 14, Zhang shows a pixel section 202 formed on substrate 201, signal line drive circuit 203, and scanning line drive circuit 204, as well as signal lines 205, formed on the pixel region 202, gate

insulating film 206 formed on each of the components 203, 204, 205, and gate electrodes 207, 208, 209 formed on the gate insulation film 206, as shown in FIG. 2A. Zhang does not teach or suggest forming gate transmitting wires on the substrate and forming a gate insulating layer over the gate transmitting wires, as set forth in amended claim 14.

The Office Action combines Zhang with Noritake et al. and Kuwashiro in rejecting claims 14 and 4, but neither of these patents cures the deficiencies of Zhang as a primary reference.

In view of the foregoing, it is respectfully submitted that independent claims 1, 6, 9, and 14 patentably distinguish over the cited art, taken alone or in combination, and reconsideration and withdrawal of the rejections under 35 U.S.C. §102(b) and 103(a) are requested. Since the remaining claims depend directly or indirectly from allowable independent claims 1 and 14, they should also be allowable for at least the reasons set forth above, as well as for the additional limitations provided by these claims. Therefore, all pending claims should be in condition for allowance.

CONCLUSION

Since the remaining patent cited by the Examiner has not been utilized to reject claims, but merely to show the state of the art, no comment need be made with respect thereto.

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. It is believed that a full and complete response has been made to the outstanding Office Action, and that the present application is in condition for allowance.

If there are any outstanding issues, however, the Examiner is invited to telephone Sam Bhattacharya, Reg. No. 48,107, at (703) 205-8000 in an effort to expedite prosecution.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,
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MARKED-UP COPY OF AMENDMENTS

IN THE SPECIFICATION:

Please **amend the paragraph beginning on page 5, line 16**, as follows:

Figures 3 and 4 illustrate a conventional TCP method. As shown, a source TCP 36 and a gate TCP **[**33**]** 34 are used to respectively connect the source and gate PCB 33 and 31 with the data and gate lines 28 and 26. The source and gate TCP 36 and **[**33**]** 34 respectively have the data and gate drive circuits (data and gate drive ICs) in themselves as shown in Figure 4. As shown in Figure 4, the data or gate drive IC 17 is installed on a polymer film 19, and the polymer film 19 is connected with the lower substrate 20 and the gate or source PCB 31 or 33 via an anisotropic conductive films 18.

Please **amend the paragraph beginning on page 12, line 8**, as follows:

As shown, adjacent to each gate pad 128 and each source pad 130, a gate dummy pad 157b and a source dummy pad 157a are formed respectively. Across the source pads 130 and the source dummy pads 157a, a first repair wire 150a is formed with an insulating layer (not shown) interposed between the pads and the repair wire. Similarly, a second repair wire 150b is formed across the gate pads 128 and the gate dummy pads **[**150a**]** 157b with the insulating layer interposed between the pads and the repair wire. The source

and gate dummy pads 157a and 157b are electrically connected via a dummy wire 137b that has the same material as the gate transmitting wires 137.

Please **amend the paragraph beginning on page 12, line 16**, as follows:

Since a mechanical impact or vibration acts on the upper substrate in the above-mentioned scribing and breaking process, open defects occur in the gate transmitting wire **[**171**]** 137 along first and second edges 161a and 161b of the upper substrate 110. For example, first and second open defects F_1 and F_2 of the last gate transmitting wire 137a occur, respectively, near the first and second edges 161a and 161b of the upper substrate 110.

Please **amend the paragraph beginning on page 18, line 7**, as follows:

Next, a gate insulating layer 190 are formed to cover the gate lines and the gate transmitting wires **[**180b**]** 137. Thereafter, not shown in Figure 16A, source and drain electrodes, and a plurality of data lines 125 (see Figure 14) will be formed on the gate insulating layer 190. The gate, source and drain electrodes are included in a switching device such as a thin film transistor (TFT).

Please **amend the paragraph beginning on page 18, line 18**, and **ending on page 19, line 1**, as follows:

In Figure 16B, between the dummy patterns 180b and the passivation layer 192, auxiliary dummy patterns 185 are interposed in shape of islands such that a first height "a" measured from the upper substrate 110 to the auxiliary dummy pattern 185 is smaller than a second height "b" measured from the upper substrate 110 to the gate transmitting wire 137. In this case, since the auxiliary dummy patterns 185 and the dummy patterns 180b absorb most of the scribing and breaking force in the scribing and breaking process, the gate transmitting wires 137 are protected from the mechanical impact or vibration of a cutting device used for the scribing and breaking process.

IN THE CLAIMS:

Please **amend claims 1, 6, 9, and 14** as follows:

1. (Amended) A liquid crystal display device comprising:

upper and lower substrates with a liquid crystal layer interposed therebetween;

a sealant between the upper and lower substrates in an area near an edge of the upper substrate;

a plurality of source and gate pads on the lower substrate;

a plurality of gate and data lines on the lower substrate, each gate line being electrically connected with the corresponding gate pad, each data line being electrically connected with the corresponding source pad;

a gate insulating layer between the gate lines and the data lines;

a source PCB and a gate PCB electrically connected with the plurality of source pads[; a gate PCB electrically connected with] and the plurality of gate pads, respectively, the source PCB and the gate PCB being formed outside the area in which the sealant is formed such that the upper substrate is not formed over the source PCB or the gate PCB; and

a plurality of transmitting wires on the lower substrate, the transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB.

6. (Amended) [The] A liquid crystal display device [of claim 5], comprising:

upper and lower substrates with a liquid crystal layer interposed therebetween;

a sealant between the upper and lower substrates;

a plurality of source and gate pads on the lower substrate;

a plurality of gate and data lines on the lower substrate, each gate line being electrically connected with the corresponding gate pad, each data line being electrically connected with the corresponding source pad;

a gate insulating layer between the gate lines and the data lines;

a source PCB electrically connected with the plurality of source pads;

a gate PCB electrically connected with the plurality of gate pads;

a plurality of transmitting wires on the lower substrate, the transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB; and

a repair wire crossing with each gate transmitting wire with the gate insulating layer interposed between the repair wire and the gate transmitting wire, wherein a specific resistance of the repair wire is below 10μΩ/cm inclusive.

9. (Amended) [The] A liquid crystal display device [of claim 5], comprising:

upper and lower substrates with a liquid crystal layer interposed therebetween;

a sealant between the upper and lower substrates;

a plurality of source and gate pads on the lower substrate;

a plurality of gate and data lines on the lower substrate, each gate line being electrically connected with the corresponding gate pad, each data line being electrically connected with the corresponding source pad;

a gate insulating layer between the gate lines and the data lines;

a source PCB electrically connected with the plurality of source pads;

a gate PCB electrically connected with the plurality of gate pads;

a plurality of transmitting wires on the lower substrate, the transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB; and

a repair wire crossing with each gate transmitting wire with the gate insulating layer interposed between the repair wire and the gate transmitting wire, wherein the repair wire includes first and second closed roofs, the first closed roof being formed along first edge of the upper substrate, the second closed roof being formed along second edge of the upper substrate.

14. (Amended) A method of fabricating a liquid crystal display device, the method comprising:

preparing first and second substrates;

forming a plurality of gate lines, gate pads, gate transmitting wires, and dummy patterns on the first substrate;

forming a gate insulating layer on the gate lines, gate pads, gate transmitting wires, and dummy patterns;

forming a plurality of data lines[,] and data pads[, and gate transmitting wires] on the gate insulating layer;

forming a passivation layer on the data lines[,] and the data pads[, and the gate transmitting wires];

forming a sealant on the first substrate;

attaching the first and second substrates;

scribing and breaking the second substrate; and

forming a liquid crystal layer between the first and second substrates.